Advanced Wafer Level Packaging of RF-MEMS with RDL Inductor

Paul Castillou, Roberto Gaddi, Rob van Kampen,
Yaojian Lin, Babak Jamshidi** and Seung Wook Yoon****
Cavendish Kinetics, 2960 North First Street, San Jose, CA 95134 USA
*STATS ChipPAC Pte. Ltd. 5 Yishun Street 23, Singapore 768442
**STATS ChipPAC Inc.46429 Landing Parkway Fremont, CA 94538 USA
***STATS ChipPAC Pte. Ltd. 10 Ang Mo Kio Street 65 Techpoint #04-08/9 Singapore 569059
Seungwook.yoon@statschippac.com

Abstract

The market for portable and mobile data access devices that are wirelessly connected to the cloud anytime and anywhere is exploding. The trend to access any network from anywhere is driving increased functional convergence in the radio, which translates into increased packaging complexity and sophistication. This is creating unprecedented demand for RF components providing more integration- in smaller package sizes. There are exciting interconnect technologies in wafer level packaging such as wafer level chip scale packaging (WLCSP) or fan-out wafer level packaging (FO-WLP) solutions such as embedded Wafer Level Ball Grid Array (eWLB) to meet these needs.

One of the most promising solutions to enable the required RF performance levels in mobile and wearable devices is the use of RF MEMS Tuners. Mobile original equipment manufacturers (OEMs) are rapidly adopting antenna tuning solutions to be able to provide the required signal strength across the large number of LTE spectrum bands used globally.

With RF MEMS technology now maturing, the biggest challenge to address the fast growing opportunity was to find a suitable packaging technology that can deliver RF MEMS tuners in the smallest possible form factor, while maintaining the excellent performance characteristics of the RF MEMS technology. After careful analysis, an eWLB/FO-WLP package was adopted and released to volume production in 2015. The commercial eWLB/FO-WLP RF MEMS tuners outperform traditional RF silicon-on-insulator (SOI) switch-based antenna tuning solutions, resulting in much higher data rates (up to 2x) and improved battery life (up to 40%). Redistribution layers (RDL) in eWLB are utilized for higher electrical performance and complex routing to meet electrical requirements. The ability to utilize embedded passives in a multi-layer eWLB structure provides a number of advantages including cost reduction, footprint reduction and increased reliability. Inductors in eWLB offer significantly better performance compared to inductors in standard on-chip technologies.

In this paper, we examine the WLCSP and eWLB packaging assembly flow, solutions to RF design challenges as well as characterization of RF performance. Further improvement of the quality factor of the integrated inductor and capacitors by using low-loss thin-film dielectrics and molding compound in eWLB will be reported as well. Package level reliability test results will also be presented in this paper.

Key words

RF-MEMS, Wafer Level Packaging, eWLB, Fanout-WLP, Embedded inductor,

I. Introduction

As a small, lightweight, high performance semiconductor package, wafer-level chip-scale packaging (WLCSP) has been a popular solution for space constrained mobile devices and is a compelling solution for new IoT and wearable electronics (WE) applications. WLCSP was introduced in the late 1990s as a semiconductor package wherein all manufacturing operations are performed in wafer form with dielectrics, thin-film metals and solder bumps applied directly on the surface of the die with no additional packaging. The WLCSP provides the smallest possible package size since—the final package is no larger than the die itself. The volume of WLCSP used in the industry has experienced steady growth – driven by the small form factor and high-performance requirements of mobile consumer products.

LTE Smartphones and their built-in antennas must support up to 40 different spectrum bands, ranging from 700 MHz up to 2.7 GHz. At the same time Smartphones are getting thinner and are made out of metal, which further impacts the antenna performance [1]. It is the primary objective of every antenna designer to maximize the 'antenna efficiency' for every spectrum band, to deliver the highest RF signal strength. RF MEMS Tuners provide unprecedented (as in really high) Q-factors that enable highest-efficiency, tunable narrow-band antennas. It needs these requirements; i) accurate and reliable so the antenna will always be tuned perfectly, ii) tiny so it can easily be attached to the smart phone antenna and iii) lossless, so RF signal strength and quality are not compromised

RF MEMS is expected to penetrate the 3G and the 4G mobile market. And increased usage of RF MEMS in smart devices is one of the major drivers of the market. Over the past few years, there has been unprecedented growth in the adoption of RF MEMS in smartphones. The demand is expected to grow as RF MEMS enable fast data transfer and enhanced network operations in smart devices. The smart phone manufactures are increasingly adopting the technology because of its size and compatibility, along with reduced cost per unit [2].

In order to meet these requirements of RF MEMS devices, advanced wafer level packaging solution is key for maximizing its performance and smaller formfactor as well as reliability for mobile products.

II. Wafer Level Packaging for RF MEMS Tuner

A. Advanced Wafer Level Packaging

For emerging applications requiring significantly more integration, a transition from fan-in WLCSP to fan-out wafer-level packaging (FOWLP) is often required to achieve maximum connection density, improved electrical and thermal performance and small package dimensions. FOWLP, also known as embedded wafer-level ball grid array (eWLB), is a versatile interconnection system processed directly on the wafer and is compatible with motherboard technology pitch requirements. Unlike fan-in wafer-level packaging, eWLB is not constrained by the semiconductor die size as shown in Fig.1.

eWLB technology addresses a wide range of factors for mobile, IoT and WE applications. At one end of the spectrum is the need for a significant increase in input/output (I/O) density, a particular challenge as packages become progressively smaller and thinner. eWLB achieves fine line width and spacing as well as superior electrical performance, providing more design flexibility and a significant reduction in size than is possible with printed circuit board (PCB) technology. eWLB also provides the ability to integrate different active and passive elements, embedded very close to each other as an SiP. Complex thermal issues related to power consumption and device's electrical performance (including electrical parasitic and operating frequency) are successfully addressed by eWLB technology [2].

On the other side of the spectrum is the need to reduce assembly and test costs to meet consumer requirements for mobile, IoT and WE. The manufacturing process for eWLB is well established and lends itself to the use of large wafer and panel sizes, which provides compelling cost reductions over conventional wafer-level processing.

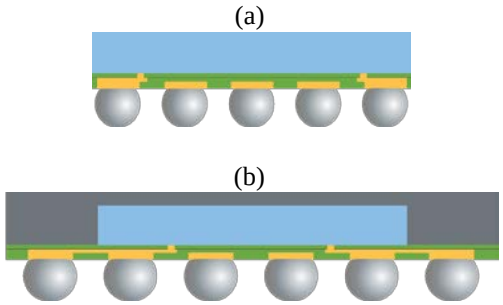

Figure 1. Schematics of wafer level packaging : (a) conventional Fan-in WLP and (b) eWLB (Fan-out WLP)

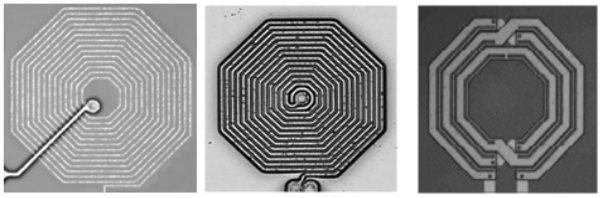

Figure 2. Thick Cu RDL inductor coils in eWLB

Redistribution layers (RDL) in eWLB as shown in Fig. 2 are utilized for higher electrical performance and complex routing to meet electrical requirements (Figure 3a). RDL also can provide embedded passives (R, L, C) using a multi-layer structure. Excellent performance of transmission lines was reported in manufacturing eWLB (insertion loss 0.1dB/mm @ 10GHz, 0.25dB/mm @ 60GHz). Inductors in eWLB offer significantly better performance compared to inductors in standard on-chip technologies. Further improvement of the quality factor of the integrated inductor and capacitors by using low-loss thin-film dielectrics and molding compound in eWLB was reported as well [3,4].

B. Inductor on Molding Compound

Fig. 3 depicts Q performance comparison of a 3.6 nH inductor made from different processes/options. As can be seen, if an inductor is made directly above an active IC through this process, its Q peak is around 26. But if made in fan-out area, its peak Q can be 35. Even compared to the same inductor made from regular IPD process [5], the Q value from the inductor made in the mold material is still the best.

The high-Q inductors made in the mold material are therefore good candidates for RF passive functional blocks. In addition, the plating Cu RDL process may remove using the specially-treated IPD substrates for low cost. If capacitors are needed in the circuits, we may still use an IPD chip to build them, but the IPD substrate can be regular p-type substrates too for low cost.

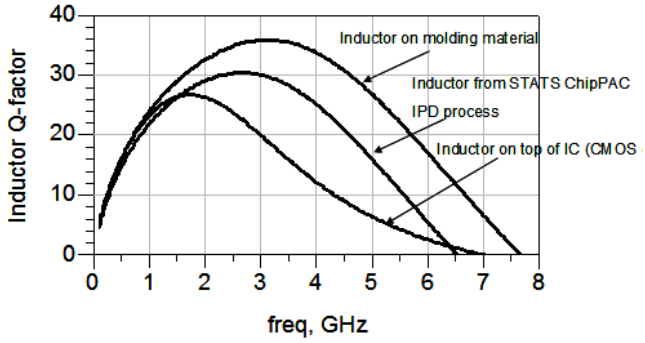

Figure 3. Q-factor comparison of inductors made from different options/processes.

III. Assembly Process

For the wafer level chip scale package (WLCSP), all manufacturing operations were done in wafer form with dielectrics, thin film metals and solder bumps directly on the surface of the die with no additional packaging [4]. Unlike conventional WLP, the first step in eWLB manufacturing is to thin and singulate the incoming wafer. The reconstitution process as shown on the left in Figure 4 includes four main steps.

1) The reconstitution process starts by laminating an adhesive foil onto a carrier.
2) The singulated die are accurately placed face down onto the carrier with a pick and place tool.
3) A compression molding process is used to encapsulate the die with molding compound while the active face of the die is protected.
4) After curing the molding compound, the carrier and foil are removed with a de-bonding process, resulting in a reconstituted wafer where the molding compound surrounds all exposed silicon die surfaces.

The eWLB process is unique in that the reconstituted wafer does not require a carrier during the subsequent wafer level packaging processes. The implementation of this process flow into 300mm diameter reconstituted wafers has been described in detail in previous presentations.

As shown in Fig. 4, Si dicing is done after wafer sort test in Conventional WLCSP. Hence, impact of chipping, side wall crack on device functionality is not assessed. In eWLB, this is done before Final Test. Hence, impact of chipping, side wall crack on device could be captured in final test. And eWLB package dicing is done in mold compound only and not in Silicon. Hence, no mechanical impact to Silicon at all.

Fig. 5 shows packages, conventional fan-in WLCSP and eWLB with thick Cu RDL inductor.

Figure 4. Process flow of WLCSP and eWLB

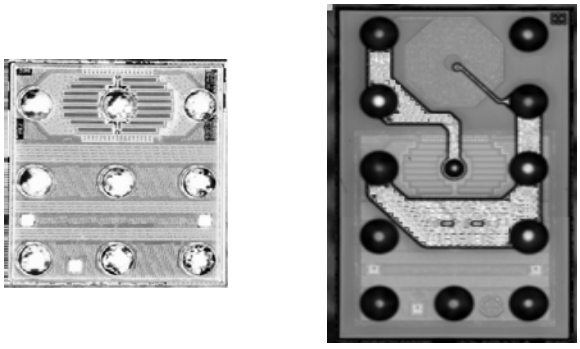

Figure 5. Assembled packages of RF-MEMS Tuner : (a)WLCSP and (b) eWLB with inductor RDL

IV. Reliability Test Results

Table 1 shows the package level reliability result of RF-MEMS WLCSP and eWLB. They passed JEDEC (Joint Electron Device Engineering Council) standard package reliability tests such as MSL (Moisture Sensitivity Level) 3 with Pb-free solder conditions. The test vehicles, WLCSP and eWLB were 1.3x1.5 and 1.6x2.5mm, respectively as shown in Fig. 5. Both packages successfully passed all industry standard package level reliability with ball shear test and OS test.

Table 2 shows board level reliability of JEDEC TCoB and drop test results of daisychain test vehicle of WLCSP and eWLB. The first TCoB failure was after 1000 cycles. Drop reliability performance was robust and showed no failure after 100 drops. These test results show the robustness of board level reliability of WLCSP and eWLB.

Table 1. Package Level Reliability Results of RF-MEMS WLCSP and eWLB.

Reliability Test	JEDEC	Test Condition	Read-out	Results
Unbiased HAST (W/ MSL3)	JESD22-A118	130°C, 85%RH	168hrs	Pass
Temperature Cycling (TC-B, w/MSL3)	JESD22-A104	-55/125°C; 2Cy/hr	1000x	Pass
High Temp. Storage (HTS)	JESD22-A103	150°C	1000hr	Pass

Table 2. Board Level Reliability Test Results of RF-MEMS WLCSP and eWLB.

Tests	Conditions	Status
TCoB	JEDEC JESD22-A103 -40°C to 125°C	Pass
Drop Test	JEDEC JESD22-B111 1500G	Pass

V. RF performance Test Results

The eWLB device of Fig 5b) contains the RF-MEMS Tuner (from Fig 5a) and a RDL inductor for enhanced tuning range and ESD protection. The inductor value has been designed so that the minimum capacitance at frequencies of interest for low-band antenna tuning (<1GHz) is reduced to half of that of the intrinsic RF MEMS tuner. The effective tuning ratio of the fully packaged RF MEMS Tuner including the inductor is therefore doubled. The intrinsic very high quality factor of the RF MEMS tuner allows to take the burden of the reduction in Q factor due to the inductor: the total Q factor of the packaged Tuner is still high enough to allow efficiency enhancements in low-band antenna tuning applications.

Figure 6 shows the 3D EM simulation results of the inductor included in the RF-MEMS package. Nominal inductance value is 65nH. The inductor Q factor is peaking to a value of 35 in the frequency range of interest for low-band antenna tuning applications.

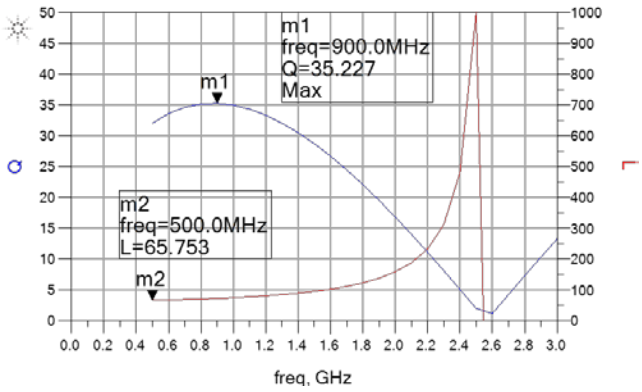

Figure 6. Q-factor and Inductance simulation results for the RDL inductor added in the RF MEMS Tuner package.

VI. Conclusion

In this work, we studied and developed WLCSP and eWLB packaging of RF MEMS tuner. Also solutions to RF design challenges were investigated as well as characterization of RF performance. Further improvement of the quality factor of the integrated inductor and capacitors by using low-loss thin-film dielectrics and molding compound in eWLB was reported. Package and board level reliability test results were presented with JEDEC conditions.

1) eWLB technology is an important wafer-level packaging solution that will enable the next-generation of a mobile, IoT and wearable applications. The advantages of standard fan-in WLPs, such as low assembly cost, minimum dimensions and height, as well as excellent electrical and thermal performance, are equally true for eWLB. The differentiating factors with eWLB are the ability to integrate passives like inductors, resistors and capacitors into the various thin-film layers, active/passive devices into the mold compound.

2) The high Q inductors made from wafer-level package using mold compounds as substrates enable high performance RF circuits through packages. This packaging process is similar to the RDL process in semiconductor industry, which can potentially provide high integration, low cost, small-form factor, high yield features for RF-MEMS Tuner device.

3) WLCSP and eWLB both passed JEDEC component and board level reliability tests.

4) Also showed improved RF performance with advanced wafer level packaging in RF characterization study.

Acknowledgement

Authors appreciated for support and help from Cavendish Kinetics engineering team and STATS ChipPAC Singapore RnD and design&characterization team.

References

[1]http://www.cavendish-kinetics.com/rf-mems-products/rf-mems-smartuners/

[2] RF MEMS market, RCR Wireless , Kelly Hill, 25 August 2015. http://www.rcrwireless.com/ 20150825 /devices/rf-mems-maker-raises-36-million-tag6

[2] Seung Wook Yoon, Boris Petrov, Kai Liu, "Advanced wafer-level technology: enabling innovations in mobile, IoT and wearable electronics" , Chip Scale Review, May/June 2015, pp54-57.(2015)

[3] Maciej Wojnowski, Klaus Pressel, Grit Sommer, Mario Engl, "Package Trends for Today's and Future mm-Wave Applications," EuMIC 2008, 38th European Microwave Conference

[4] M. Wojnowski1, M. Engl, B. Dehlink, G. Sommer, M. Brunnbauer, K. Pressel, and R. Weigel, "A 77 GHz SiGe Mixer in an Embedded Wafer Level BGA Package," Proceedings of 50th ECTC, p.290-296, May 2008, (2008)

[5] *IPD Products Databook* (Second Edition), STATS ChipPAC's website.

http://www.statschippac.com/packaging/packaging/waferlevel/ipd/ipd%20library.aspx